



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln No.: 10/021,736

Filed: October 30, 2001

Applicant(s): Malcolm Whitlock

Title: METHOD AND APPARATUS FOR
MEASUREMENT OF JITTER

Art Unit: 2637

Examiner: Jacob M. MEEK

Attorney Docket No.: 72404

Customer No.: 22242

Confirmation No. 1061

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Commissioner for Patents
P.O. Box 1450
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Dear Sir:

A claim for priority based on United Kingdom Patent Applications No. 0026556.1 is filed herewith for the above-identified U.S. application. Enclosed, in compliance with 37 C.F.R. §1.55, is a certified copy of the United Kingdom Priority Document filed October 31, 2000.

Respectfully submitted,

Date: February 3, 2006

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Statement of inventorship and right to grant of a patent (Patents Form 7/77)

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Request for preliminary examination and search (Patents Form 9/77)

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Request for substantive examination (Patents Form 10/77)

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11.

I/We request the grant of a patent on the basis of this application.

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Peter D. Hudson

Date

30 October 2000

12. Name and daytime telephone number of person to contact in the United Kingdom

Peter Hudson

01420 562568

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1. Your reference

00.0124-con/pdh

2. Patent application number

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0026556.1

3. Full name, address and postcode of the or of each applicant (underline all surnames)

Consultronics Europe Limited
Omega Enterprise Park, Electron Way,
Chandlers Ford, Hampshire, SO53 4SE

Patents ADP number (if you know it)

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

08011991001

4. Title of the invention

METHOD AND APPARATUS FOR MEASUREMENT OF JITTER

5. Name of your agent (if you have one)

~~Peter Hudson~~

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5/17
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Number of earlier application

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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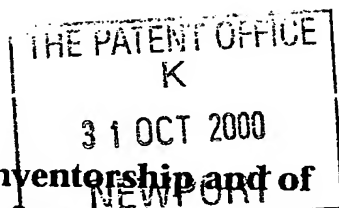
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The Patent Office

31 OCT 2000

Cardiff Road
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1. Your reference 00.0124-con/pdh

2. Patent application number
(if you know it) 0026556.1

3. Full name of the or of each applicant Consultronics Europe Limited

4. Title of the invention METHOD AND APPARATUS FOR MEASUREMENT OF
JITTER

5. State how the applicant(s) derived the right
from the inventor(s) to be granted a patent Invented during inventor's employment by applicant,
as part of normal duties of employment

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Signature

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Peter D. Hudson

30 October 2000

8. Name and daytime telephone number of
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METHOD AND APPARATUS FOR MEASUREMENT OF JITTER

Field of the Invention

5

This invention relates to measuring the amount of jitter present on a digital signal. Ideally, in a digital signal transitions between different levels occur at precise times; however, in practice the actual time at which a transition occurs may vary slightly from the ideal. Such variations are commonly referred to as jitter.

15 Background of the Invention

In the field of this invention it is known that the normal method of measuring jitter is to use an analogue based system implemented with a Phase Locked Loop (PLL) which tracks the input signal, therefore resulting in the PLL's oscillator control voltage containing imposed thereon an analogue representation of the jitter component of the input signal. This PLL oscillator control voltage signal can then be filtered and its level can be displayed. However, such an approach is subject to the disadvantages inherent in analogue circuitry, such as high cost, difficulty in achieving desired accuracy of performance through need to match exact performance of analogue components and lack of performance stability over changes in temperature and time.

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Another method (known from patent publication WO 99/57842) of measuring jitter, using a digital approach, is to track the incoming signal with a PLL, to produce a very low frequency offset (e.g., 1.27 parts per million (ppm) and to count the number of coincidences of phasing for each sample period together with the time between these coincidences.

However, this approach requires separate analogue circuitry, a phase locked loop and jitter attenuator, and the input signal frequency needs to be tracked by this PLL with an extremely small offset (1.27 ppm) in order to work.

A need therefore exists for an apparatus and method for measurement of jitter wherein the abovementioned disadvantage(s) may be alleviated.

Statement of Invention

In accordance with a first aspect of the present invention there is provided a method for measurement of jitter as claimed in claim 1.

In accordance with a second aspect of the present invention there is provided an apparatus for measurement of jitter as claimed in claim 7.

It will be understood that the invention allows measurement of jitter in a digital signal without need for high frequency clocking, Phase Locked Loops (PLLs) or

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similar analogue circuitry. This enables it to be implemented completely within a Field Programmable Gate Array (FPGA) with the need of just an external programmable oscillator.

5 It will be further understood that the invention does not rely on having to track the input signal accurately, and although it may require the ability to measure the frequency of the input signal this can be performed using
10 a simple frequency counter (e.g., within the FPGA).

Brief Description of the Drawings

15 One method and apparatus for measurement of jitter incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

20 FIG. 1 shows a flow chart illustrating the method for measurement of jitter;

FIG. 2 shows a digital signal waveform diagram illustrating the absence of jitter;

25 FIG. 3 shows a digital signal waveform diagram illustrating the presence of jitter; and

30 FIG. 4 shows a block schematic diagram of a circuit for measurement of jitter using the method of FIG. 1.

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Description of Preferred Embodiment

In essence, the preferred embodiment of the present
5 invention utilizes a technique in which a programmable
oscillator (reference clock) runs at a slightly different
frequency (offset) to the incoming signal so that the
phase of the two clocks drift over time, enabling
10 detection of jitter in the input signal by measurement of
the difference in the number of clock cycles it takes for
this drift to occur.

A frequency counter is used to measure the frequency of
the input signal and then the programmable oscillator
15 (reference clock) is set to a frequency with a fixed
offset. If the input frequency is exactly 2,048,000 Hz
then setting the programmable oscillator to 2,027,723 Hz
(100/101) times this frequency would take 100 reference
clocks (101 input signal clocks) for the signals to
20 change phase by exactly 100%. Any jitter present on the
input signal would cause a change in the number of clock
cycles required for this phase change. Because the
jitter can have a wideband frequency component it is
necessary to perform multiple measurement cycles, for a
25 single test, all based on the original reference point to
catch the peaks of the jitter component.

This technique detects a phase match and then from the
calculated offset frequency determines the exact number
30 of clock cycles required to the next phase match for a
jitterless signal. Using this calculated value, many
cycles are performed and if jitter is present then for

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each cycle the number of clock pulses required to reach a phase match will be different. It is also important to understand that as these cycles are referenced to just the first phase match and not subsequent matches, the phase match at the start of each cycle will not occur in the same place; therefore a cycle counter must not be reset to these matches but to the calculated position.

By storing maximum and minimum values in the counter when a phase match is detected the total phase variation can be calculated at the end of the test. When very high frequency jitter is present many phase matches will be detected within each measurement cycle; however, they are all valid and therefore the first (minimum) and last (maximum) must be stored. As there will be jitter all through the input signal, the beginning of the measurement cycle will also have phase matches occurring at different positions and these need to be blocked so that they do not effect the stored maximum and minimum values.

Referring now particularly to FIG. 1, the method based on the above technique involves two main timing cycles:

1. The measurement cycle set by the frequency offset; this is 200 clock cycles for the above example but can be any value that suits the resolution of the jitter to be measured. This is set to twice the actual phasing period so that excursions greater than the calculated value can be captured.

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2. The test cycle, which determines the low cutoff frequency of the measurement, which is a multiple of the phase repetition cycle.
- 5 After start (step 102) of the method, the frequency (e.g., 2,048,000 Hz) of the input signal (whose jitter is to be measured) is measured and the offset frequency (e.g., 2,027,723 Hz) is calculated and an appropriate reference clock signal is produced at this offset
10 frequency (step 104).

To measure the peak maximum and peak minimum jitter two registers (MAX and MIN) are used, and at the start of the jitter measurement the MAX register is reset to zero and
15 the MIN register is set to its maximum possible reading (step 106). A phase match 'wait loop' (step 108) is then followed until a phase match occurs, i.e., until both the input signal and the reference clock are exactly in phase (this match may conveniently be performed by detecting
20 the coincidence of the rising edge of both the input signal and the reference clock, but it will be understood that 'falling edge' or other methods of phase comparison may alternatively be used).

- 25 Two counters, a measurement counter and a test cycle counter, are reset to zero and begin incrementing by the reference clock signal (step 110). Each time the reference and input signals are again exactly in phase (step 112), if the sample is not blocked (step 114, which
30 will be explained in more detail below) the value in the measurement counter is compared with the values in the MAX and MIN registers. If the measurement counter value

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is higher than the value in the MAX register (step 116), the MAX register is updated (step 118); and if the measurement counter value is lower than the value in the MIN register (step 120), the MIN register is updated (step 122). This ensures that each time phase coincidence occurs the minimum and maximum excursions are retained.

As mentioned above, a blocking pulse is produced (step 114) so that any phase match at or near to the start/end of the test cycle is not detected. For the example described above where the test cycle is 200 clocks the blocking pulse would only allow coincidence occurring between say clock cycles 50 and 150 to update the MAX & MIN registers. The measurement counter continues to increment, being reset to zero when it reaches its calculated limit (step 124) as many times as defined by the test cycle to give the required low frequency cutoff.

When the measurement cycle counter reaches twice the calculated phasing position (step 126), it is reset (step 128) and the next measurement cycle begins. This allows for MAX (positive peak) jitter to be detected which will be later than the expected position. It is important that each measurement cycle is referenced to the original phase coincidence and not reset; otherwise both high and low frequency limits would be imposed. To overcome the possibility of not being able to detect fixed frequency jitter based on a frequency that would beat with the offset frequency, the offset frequency can be changed between test cycles if necessary.

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The final values are then read from the MAX and MIN registers (step 130), and the total peak-to-peak jitter is calculated by subtracting the value in the MIN register from the value in the MAX register and dividing this difference by the calculated number of clock cycles between phase matches. Ultimately, the method ends at step 132.

FIG. 2 shows how the phasing affects the MAX and MIN registers in the presence of a jitterless signal.

FIG. 3 shows how jitter would affect the MAX and MIN registers.

As can be seen from FIG. 2, if no jitter is present then following the first phase match (causing the starting of the test) at point 202 between the input signal 204 and the reference signal 206, the next coincidence (causing possible updating of the MAX and MIN registers) will always be at the same point 208 and both registers will have the same number (100 for the example above). As can be seen from FIG. 3, if jitter is present then following the first phase match (causing starting of the test) at point 302 between the input signal 304 and the reference signal 306, different numbers will be stored in the MAX and MIN registers: the MIN register will be updated at point 308, and the MAX register will be updated at point 310. The difference between these numbers will be the peak-to-peak amount of jitter in steps equal to the reciprocal of the ratio of the frequency offset, 0.01 (1/100) Unit Intervals (UI) for the above example.

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It will be understood that this example limits the technique to being able to measure no more than 1 UI (± 0.5 UI). It will equally be understood that this limitation may be removed by pre-scaling the input signal with a divider. For example, if the input signal is first divided by 8 (the particular value of this number is not important other than to extend the range) then the method of measurement would have a capability of reading up to 8 UI (± 4 UI) with the resolution being reduced to $8/100$, i.e., 0.08 UI, steps however this reduction can be removed by changing the frequency offset by the same scaling factor.

Similarly, it will be understood that the particular value of the frequency offset is not important for the basic functionality of the technique and can be changed to suit the required resolution.

Referring now to FIG. 4, test equipment 400 includes a circuit 401 for measuring, using the method described above, the jitter present on a digital signal of a telecommunications pulse code modulation (PCM) link.

The circuit 401 includes a frequency counter 402 arranged to receive an input digital PCM signal I whose jitter is to be measured. The frequency counter 402 has an output connected to a microprocessor (or microcontroller) 403, which controls a programmable oscillator 404.

The programmable oscillator 404 has an output that is connected to one input of a phase comparator 405, of which another input is arranged to receive the input

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digital PCM signal I . A 'phase match' output of the phase comparator 405 is connected to the input of a counter 406, which is arranged to be connected to receive as its clock input the output signal C_{REF} from the programmable oscillator 404. The counter 406 has an output that is connected to the input of a test cycle counter 407, of which an output is connected to reset the counter 406.

An output of the counter 406 is connected to one input of a maximum comparator 408 and to one input of a minimum comparator 409. A blocking window generator 410 is connected to receive outputs from the phase comparator 405 and from the counter 406, and has an output that is connected to enable comparisons in the maximum comparator 408 and in the minimum comparator 409.

A maximum register 411 is connected to receive at one input thereof the output of the maximum comparator 408. A minimum register 412 is connected to receive at one input thereof the output of the minimum comparator 409. The maximum register 411 and the minimum register 412 have respective reset inputs, which are connected to receive a 'reset registers' signal from the output of the test cycle counter 407. The maximum register 411 has an output, for producing a 'maximum output' signal O_{MAX} , which is connected to another input of the maximum comparator 408. The minimum register 412 has an output, for producing a 'minimum output' signal O_{MIN} , which is connected to another input of the minimum comparator 409.

As referred to in the discussion of the method above, a pre-scaling divider 413 may be used to divide the input

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signal I by a desired value so as to increase measurement resolution.

In use of the circuit 401 of the test equipment 400, the
5 frequency of the input signal I is measured by the
frequency counter 402 and this measurement is fed to the
microprocessor 403. The microprocessor 403 calculates a
frequency offset (as will be described in more detail
below) and sets the programmable oscillator 404 to
10 produce at its output a reference clock signal C_{REF} of
this calculated offset frequency. The microprocessor 403
also controls resetting of the counters, including the
test cycle counter 407 (which in turn controls resetting
of the maximum register 411 and the minimum register
15 412), and reads the final values in the maximum and
minimum registers; however, for the sake of clarity,
links illustrating these functions have been omitted from
FIG. 1.

20 At the start of a measurement cycle, the maximum register
411 is set to zero and the minimum register 412 is set to
its maximum possible value (which is greater than twice
the phase repeat cycle). Both the counter 406 and the
test cycle counter 407 are held in reset until a first
25 phase match is detected. When the phase comparator 405
detects an exact phase match (between the input signal I
and the reference clock signal C_{REF}) the counter 406 and
the test cycle counter 407 are started. Both the counter
406 and the counter 407 increment on each pulse of the
30 reference clock signal C_{REF} .

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Every time a phase match is detected in the phase comparator 405, if the blocking window generator 410 allows, the instant value of the counter 406 is compared (in the maximum comparator 408 and the minimum comparator 409 respectively) with the maximum register 411 and the minimum register 412. If the value of the counter 406 is greater than the stored value in the maximum register 411, then the maximum register 411 is updated; if the value of the counter 406 is less than the stored value in the minimum register 412, then the minimum register 412 is updated. The blocking window generator 410 only allows matches in the middle of the detection range to update the registers, ensuring that multiple phase matches occurring near the start and end of a measurement cycle are ignored.

When the counter 407 reaches the end of a measurement cycle (twice the calculate number of clocks between phase matches), the counter 406 is reset by the test cycle counter 407 and the next measurement cycle starts. The values in the maximum register 411 and the minimum register 412 are retained and only updated if the comparators deem it necessary as stated above.

This process continues with the counter 406 being reset each calculated measurement cycle by the test cycle counter 407 until the completion of the entire test, when the counter 406 is held in reset by the test cycle counter 407 and the microprocessor 403 can read the final values in the maximum register 411 and the minimum register 412. The total peak-to-peak jitter is calculated by the microprocessor subtracting the value in

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the minimum register 412 from the value in the maximum register 411 and then dividing this difference by the calculated number of clock cycles between phase matches.

- 5 As each measurement cycle is started at the calculated phasing point of the input signal, the jitter imposed on the input signal will "move around" this point and over the entire test period the maximum jitter and peak-to-peak jitter will be detected.

10

It will be understood that the method and apparatus for measurement of jitter described above provide the following advantages:

- 15 • It does not require analogue circuitry, and because the frequency offset can be large and still function, the reference frequency can be produced by a programmable oscillator. In contrast, the prior art approach of patent publication WO 99/57842 needs
- 20 to measure both the number of sampling times and the time between them to get both a course reading and a fine reading, whereas the present technique produces a direct reading from two counters (MAX and MIN) which give the peak positive and peak negative
- 25 jitter measured from the start point of the test.
- With the exception of the programmable oscillator and microprocessor the entire circuit can be implemented within a FPGA (reducing cost and
- 30 increasing reliability), although it is not necessary to do so.

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- The technique does not rely on having to track the input signal accurately, and although it requires the frequency of this signal to be measured in order to calculate the offset frequency this measurement can be performed using a simple frequency counter within the FPGA.
- The technique does not require any parts that are designed to operate at a specific frequency (such as a jitter attenuator or phase locked loop) and therefore this technique can operate over an extremely wide frequency range, limited only by the upper limit of the digital circuitry and the programmable range of the oscillator.

It will be understood that if desired modifications may be made to the examples described above, without departing from the present invention. For example, The programmable oscillator 404 could be replaced by a phase locked loop to produce the frequency offset however this would require analogue circuitry and a jitter attenuator to remove the jitter introduced by the PLL. This would also mean that if the offset and the jitter were to beat then errors would be introduced in the readings.

Further, it will be understood that rather than producing two values (maximum and minimum) of jitter as described above, it is possible to extrapolate the peak-to-peak jitter value from just one value, giving just the peak positive value or peak negative value, but this would reduce the accuracy.

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It will further be appreciated that if the invention is to be used at only one frequency which is very accurately produced, then the programmable oscillator could be replaced by a fixed frequency source with a preset
5 offset; however, this would produce errors and restrict the low frequency limit if the input signal was not exactly at the right frequency.

Other possible modifications may occur to person of
10 ordinary skill in this art without departing from the scope of the present invention.

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Claims

1. A method for measuring jitter in a digital input
5 signal, the method comprising:
producing a digital reference signal having a
predetermined frequency offset from that of
said digital input signal;
detecting a first occurrence of a predetermined
10 phase relationship between said digital input
signal and said digital reference signal;
detecting subsequent occurrence of said
predetermined phase relationship between said
digital input signal and said digital reference
15 signal; and
determining the time difference between said first
occurrence and said subsequent occurrence,
whereby to determine a measurement of jitter
present in said digital input signal.
20
2. The method of claim 1 wherein the step of producing
said digital reference signal comprises:
measuring the frequency of said digital input signal
to produce a frequency measurement; and
25 using the frequency measurement to produce said
digital reference signal having a frequency
which is offset therefrom by a predetermined
amount.
- 30 3. The method of claim 1 or 2 wherein the step of
detecting a first occurrence of a predetermined phase
relationship between said digital input signal and said

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digital reference signal and the step of detecting subsequent occurrence of said predetermined phase relationship between said digital input signal and said digital reference signal comprise detecting coincidence
5 of similar edges of said digital input signal and said digital reference signal.

4. The method of claim 1, 2 or 3 wherein the step of detecting subsequent occurrence of said
10 predetermined phase relationship between said digital input signal and said digital reference signal comprises:
detecting over a plurality of said subsequent occurrences a maximum time difference value and
15 a minimum time difference value; and
determining from said maximum time difference value and said minimum time difference value a total peak-to-peak jitter measurement.

20 5. The method of claim 4 wherein said predetermined frequency offset is varied between test cycles to facilitate detection of fixed frequency jitter based on a frequency that would beat with a fixed frequency offset.

25

6. The method of any preceding claim further comprising pre-scaling the digital input signal to increase the resolution of jitter measurement.

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7. An apparatus for measuring jitter in a digital input signal, the apparatus comprising:

receiving means for receiving a digital input signal;

5 reference signal means for producing a digital reference signal having a predetermined frequency offset from that of said digital input signal;

10 phase detecting means for detecting a first occurrence of a predetermined phase relationship between said digital input signal and said digital reference signal and subsequent occurrence of said predetermined phase relationship between said digital input signal and said digital reference signal; and
15 determining means for determining the time difference between said first occurrence and said subsequent occurrence, whereby to determine a measurement of jitter present in
20 said digital input signal.

8. The apparatus of claim 7 wherein said reference signal means comprises:

25 measuring means for measuring the frequency of said digital input signal to produce a frequency measurement; and

signal producing means for producing from said frequency measurement said digital reference signal having a frequency which is offset
30 therefrom by a predetermined amount.

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9. The apparatus of claim 8 wherein said measuring means comprises a frequency counter.

10. The apparatus of claim 8 or 9 wherein said signal
5 producing means comprises a programmable oscillator.

11. The apparatus of any one of claims 7-10 wherein said
phase detecting means comprises edge detecting means for
detecting coincidence of similar edges of said digital
10 input signal and said digital reference signal.

12. The apparatus of any one of claims 7-11 wherein said
phase detecting means comprises:

15 minimum/maximum detecting means for detecting over a
 plurality of said subsequent occurrences a
 maximum time difference value and a minimum
 time difference value; and
 jitter determining means for determining from said
 maximum time difference value and said minimum
20 time difference value a total peak-to-peak
 jitter measurement.

13. The apparatus of claim 12 wherein said
minimum/maximum detecting means comprises:

25 counter means driven by said reference signal;
 maximum register means for holding a value in said
 counter means when said phase detecting means
 detects a said second occurrence;
 maximum comparator means for comparing a value in
30 said maximum register means with a value in
 said counter means when said phase detecting
 means detects a said subsequent occurrence and

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if said counter means value is greater than said maximum register means value storing said counter means value in said maximum register means;

5 minimum register means for holding a value in said counter means when said phase detecting means detects a said subsequent occurrence; and
minimum comparator means for comparing a value in
10 said minimum register means with a value in said counter means when said phase detecting means detects a said second occurrence and if said counter means value is less than said minimum register means value storing said counter means value in said minimum register
15 means.

14. The apparatus of any one of claims 7-13 wherein the apparatus is substantially comprised in a field programmable gate array.

20 15. The apparatus of any one of claims 7-14 wherein the apparatus is arranged to sense jitter in a telecommunications pulse code modulation (PCM) signal.

25 16. The apparatus of any one of claims 7-15 wherein said predetermined frequency offset is varied between test cycles to facilitate detection of fixed frequency jitter based on a frequency that would beat with a fixed frequency offset.

30 17. The apparatus of any one of claims 7-16 further comprising pre-scaling means for pre-scaling the received

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digital input signal to increase the resolution of jitter measurement.

18. A method for measuring jitter in a digital input
5 signal substantially as hereinbefore described with
reference to the accompanying drawings.
19. An apparatus for measuring jitter in a digital input
signal substantially as hereinbefore described with
10 reference to the accompanying drawings.

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Abstract

METHOD AND APPARATUS FOR MEASUREMENT OF JITTER

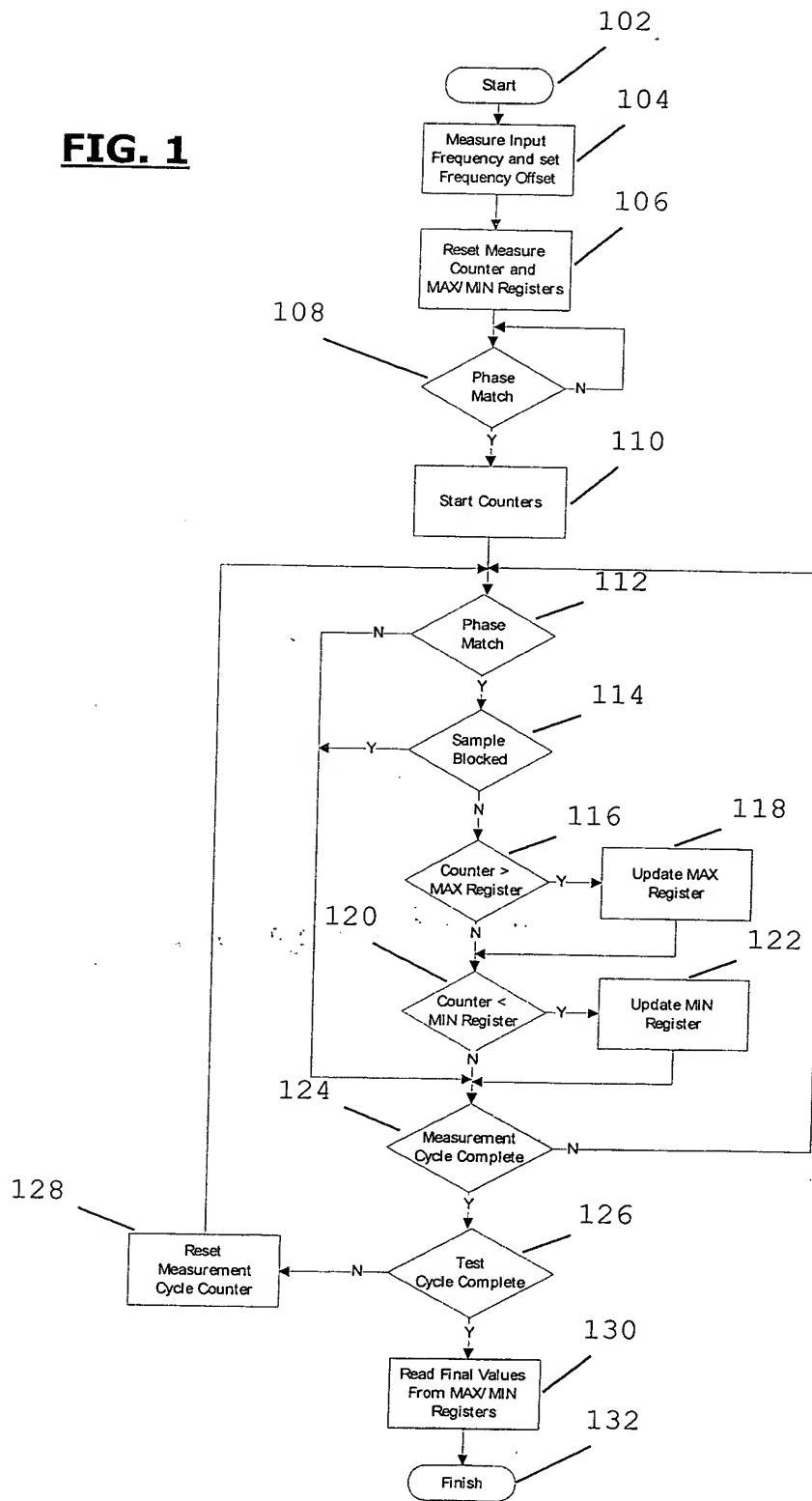
5

A method and circuit for measurement of jitter in which a reference clock (404) runs at a frequency offset to the incoming signal (I) so that the phase of the two clocks drift over time, enabling detection of jitter in the input signal by measurement of the difference in the number of clock cycles it takes for this drift to occur.

This design provides the following advantages:

- 15 • It does not require analogue circuitry and, because the frequency offset can be large and still function, the reference frequency can be produced by a programmable oscillator.
- 20 • With the exception of the programmable oscillator the entire design can be implemented within an FPGA.
- It requires no parts (such as a jitter attenuator or phase locked loop) designed to operate at a specific frequency and therefore this design can operate over an extremely wide frequency range.

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FIG. 1

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FIG. 2

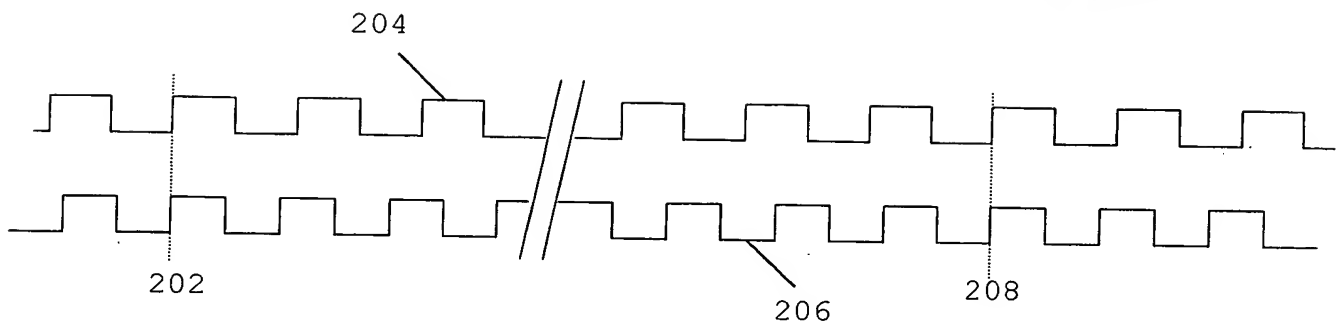
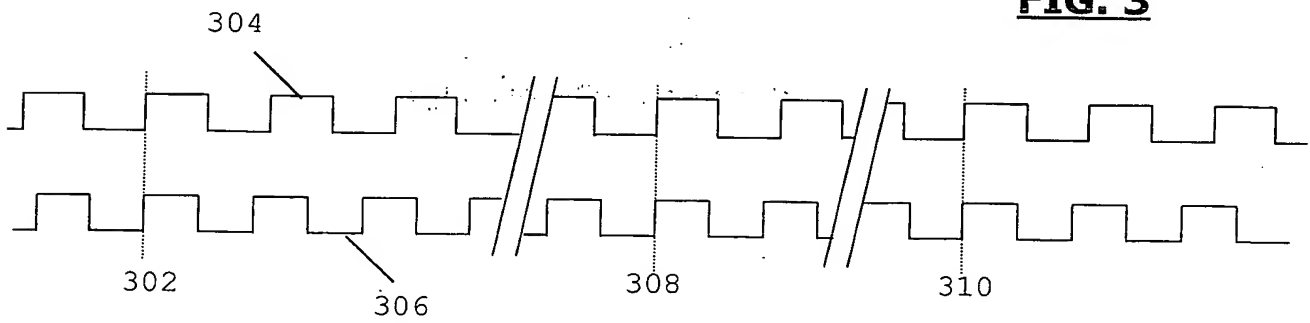
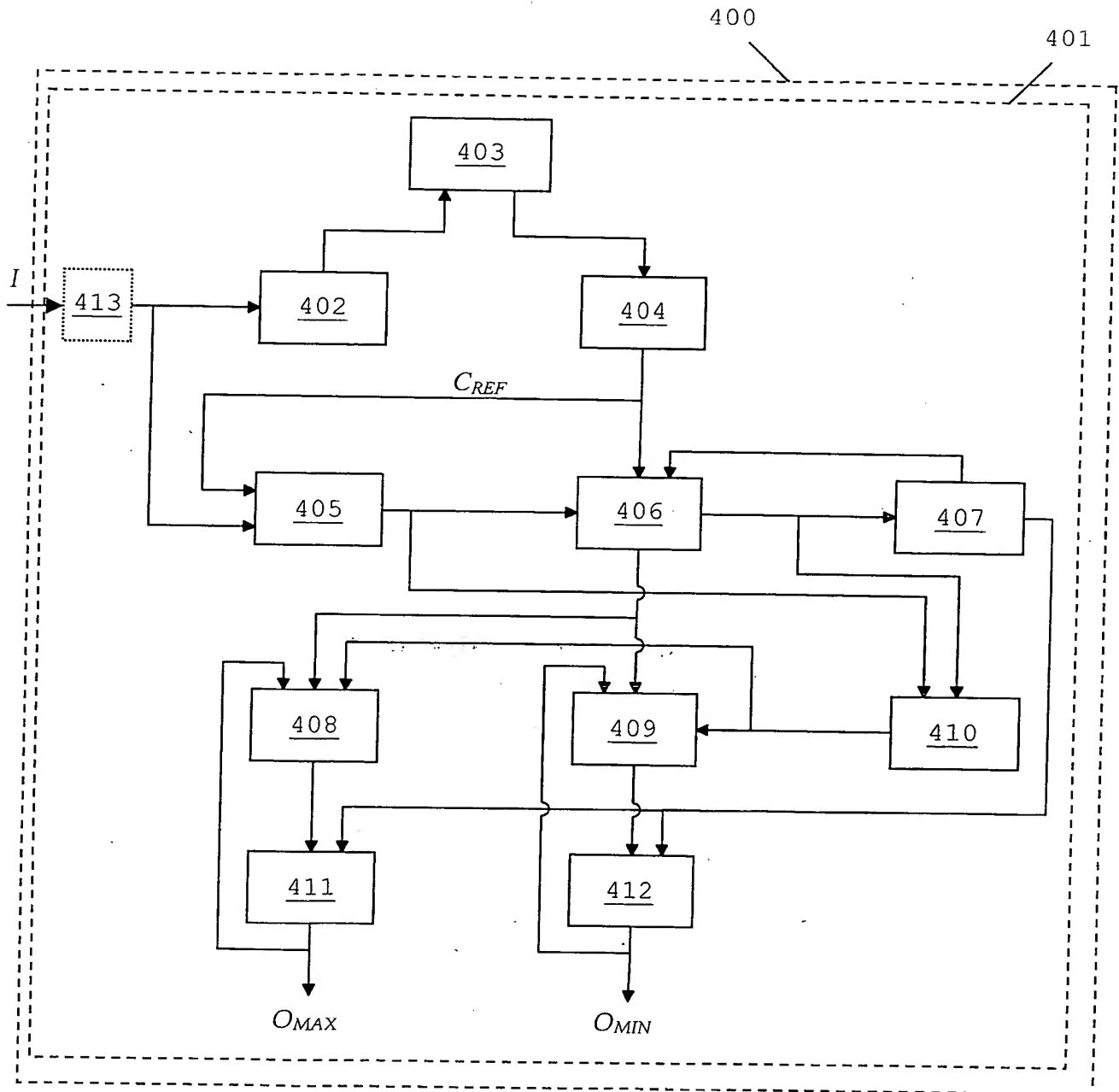


FIG. 3



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FIG. 4

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